REMARKS

Claims 1-8 and 10-19 are currently active.

The Examiner has objected to Claims 10-19. These claims now depend on Claim 8.

The Examiner has rejected Claims 8 and 10-19 under 35 U.S.C. 101. Claim 8 has been amended to include the limitation of "stored on a computer-readable medium" as the Examiner suggests to obviate this rejection.

The Examiner has rejected Claims 1-5 as being anticipated by Abramson. Applicants respectfully traverse this rejection. It is respectfully submitted that the Examiner is misapplying the term "Master abort" as taught by Abramson. Abramson does not teach or suggest anywhere that the master unit has failed let alone for the master unit to automatically recover and restart when a slave unit fails which has caused the master unit to fail.

Referring to Abramson, there is disclosed a method and apparatus for management of peripheral devices coupled to a bus. In pertinent part, Abramson teaches that if the peripheral target device will not respond, the bridge circuit 33 will perform an abort,

such as a Master abort in a PCI architecture. During such a process, the bridge circuit will disassert the I R D Y # signal line and return the bus to an idle state so that is available for use by another bus master device. In executing a Master abort, the bus master must set its Master abort detected bit in its configuration status register. See column 5, lines 55-66. Accordingly, this definition of a Master abort taught by Abramson does not indicate or mention at all, and has nothing of all to do with the master unit failing. What this teaching of Abramson indicates is that the master unit cannot communicate with the peripheral target device which causes the Master abort.

Abramson teaches several examples of how a Master abort occurs, and none of these teach or suggest the master unit has failed. Abramson teaches that if, for example, an audio device is operating in a low power mode than the access by the master component will end in a Master abort condition and an interrupt will be generated. The master component will have the physical address of the peripheral device, and once the CPU has determined that the master initiated the transfer that ended in a Master abort, the CPU can determine the physical address of the peripheral device via information stored in the master. If the Master abort did not occur in the bridge circuit, the operation of the code then turns to block 110 where a snooping operation is performed to determine which bus master received the Master abort. Control then passes to block 111b where the operation of the code attempts to determine which peripheral device failed to respond to the bus master initiated transaction.

See column 7, lines 18-50. As is clearly evident, nowhere does the master unit fail, or is even suggested to have failed when the peripheral device failed.

In another example, Abramson teaches when a notebook computer is removed from a docking station, program registers will be set to indicate a broken connection between the bus master and peripheral device. Control then passes to block 119, where a message is output to the user to indicate that the access to the device failed. If the CPU identified the cause of the Master abort condition, control passes to blocks 117 and 118 where the operation of the code interacts with the operating system by passing the information as to cause an improperly operating peripheral device. See column 8, lines 3-14. Again, from this teaching of Abramson, it clearly shows that a Master abort condition simply occurs when the broken connection is created. Nowhere is there any teaching or suggestion that the docking station has failed or any aspect of anything has failed except that the docking station cannot communicate with the notebook computer because the notebook computer has been removed from the docking station.

In the response to Arguments section on page 9 of the Office Action, the Examiner explains that in column 5, lines 55-59, Abramson discloses in a DDMA system if the peripheral target device will not respond, the bridge circuit 33 will perform an abort, such as a master abort in a PCI architecture. Abramson discloses when one of the slave devices

fails to respond, it causes a master abort (i.e. master bus terminating abnormally due to the failed slave unit).

In response, it is respectfully submitted by applicants that the Examiner is reading teachings into column 5, lines 55-59 that are not there. Specifically, in column 5, lines 59-64, Abramson teaches the definition of a master abort. Abramson teaches that "during such a process the bridge circuit 33 will deassert the IRDY # signal line and return the bus to an idle state so that it is available for use by another bus Master device". Accordingly, Abramson specifically teaches that in the master abort, the master unit does not fail but instead the signal line will be deasserted or released and the bus is returned to an idle state so that it is available for use by another bus Master device. The only device that has failed is the peripheral target device, not the bus Master device. In fact, not only does Abramson not teach that the bridge circuit 33 (or the bus Master in question) has failed, but Abramson actually teaches that when the signal line is deasserted, it is the bus that is returned to an idle state so that it can be used by another bus Master device. Applicants' claimed invention is directed specifically to the master unit, and only the master unit. When the master unit fails, it recovers and is restarted so it can continue. In contrast, Abramson teaches for another bus Master device to step in and use the signal line that was released from the peripheral target device that did not respond.

To further emphasize the distinction of applicants' claimed invention with Abramson, and to make it clear that it is the master unit that has failed or shutdown, the limitation of restarting the master unit has also been added to the claims. Antecedent support for this limitation is found on page 6, line 14 of the above-identified patent application. In other words, applicants' claimed invention specifically has the limitation that it is the master unit itself that automatically recovers and restarts after it fails. It is not the connection that has failed as Abramson suggests in regard to the line signal, or the response itself that has failed or just the peripheral target device or a slave unit that has failed, all of which are distinct from the master unit itself failing. To reiterate, a master abort specifically is taught by Abramson to mean the bus master or bridge circuit 33 deasserts the signal line to the peripheral target device and returns the bus to an idle state so that it is available for use by another bus master device. Accordingly, Abramson does not teach or suggest applicants' claimed invention.

Accordingly, Abramson does not teach or suggest the limitation of "a software program that causes the master unit to automatically recover and restart when a slave unit fails which has caused the master unit to fail and to avoid further accessing the failed slave unit," as found in Claim 1, and Claim 1 is patentable over Abramson.

Claims 2-5 are dependent to parent Claim 1 and are patentable for the reasons Claim 1 is patentable.

The Examiner has rejected Claims 6-8 and 10-19 as being unpatentable over Abramson in view of Cepulis. Applicants respectfully traverse this rejection. As explained above, Abramson fails to teach or suggest the limitation of "automatically recovering the master unit which has failed because the failed slave unit failed," as found in Claim 6. Cepulis does not teach or suggest this limitation either. The Examiner cites Cepulis simply for the supposed teaching that the master unit is directed to avoid further accessing the failed slave unit. Accordingly, Claim 6 is patentable over the applied art of record. Claim 7 is dependent to Claim 6 and is patentable for the reasons Claim 6 is patentable.

Claim 8 is patentable over the applied art or record for the reasons Claim 6 is patentable. Claims 10-19 are dependent to parent Claim 8 and are patentable for the reasons Claim 8 is patentable.

In regard to Claim 2, there is the limitation of persistent storage that survives across abnormal termination of the master unit. The Examiner cites the main memory 35 in figure 2 for meeting this limitation. However, a review of the main memory 35 and the text says nothing about the main memory being persistent storage let alone that it survives across abnormal termination of the master unit. The memory 35 can be a different type of memory, which is not persistent storage, and which have nothing at all to do with abnormal termination of the master unit, let alone surviving abnormal termination of the master unit. Accordingly,

Claim 2 is additionally patentable over the applied art of record. Claim 10 is patentable for the reasons Claim 2 is patentable.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-8 and 10-19, now in this application be allowed.

Respectfully submitted,

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